



## VACUUM PACKAGE FABRICATION OF INTEGRATED CIRCUIT COMPONENTS

### TECHNICAL FIELD OF THE INVENTION

This invention relates generally to integrated circuit fabrication and, more particularly, to a system and method for vacuum package integrated circuit component lids, or similar devices, used during fabrication of vacuum-packaged circuit components.

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### BACKGROUND OF THE INVENTION

Microelectromechanical systems (MEMS) are integrated micro devices or systems combining electrical and mechanical components. MEMS devices may be fabricated using standard integrated circuit batch processing techniques and may have a variety of applications including sensing, controlling, and actuating on the micro scale. MEMS devices may function individually or in arrays to generate effects on a macro scale.

Many MEMS devices benefit from a vacuum environment in order to obtain maximum performance. The vacuum package also provides protection and an optimal operating environment for the MEMS device. Examples of these MEMS devices are infrared MEMS such as bolometers and certain inertial MEMS such as gyros and accelerometers. Currently MEMS devices are individually packaged in vacuum-compatible packages after fabricating and dicing of the MEMS device. Under current packaging methods, the packaging costs of MEMS devices can be as much as ten to one hundred times the fabrication costs. These high packaging costs make it difficult to develop commercially-viable, vacuum-packaged MEMS devices.

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### SUMMARY OF THE INVENTION

Lid wafers and device wafers are often mated and sealed using solder, adhesive, or compression methods that result in excess sealing material being deposited within the area occupied by a MEMS device, integrated circuit, infrared detector, or other devices contained within mated lid wafers and device wafers. This excess material may exist because of the desirability of a complete and airtight seal between the device wafer and lid wafer. Accordingly, more sealing material than is required for an effective seal may be deposited between the lid wafer and device wafer. When the device wafer and lid wafers are mated, the excess sealing material may invade the resulting cavity and interfere with

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the operation of the MEMS device, integrated circuit, infrared detector, or other device enclosed therein.

Among other things, various embodiments of the present invention address the problem of excess solder, adhesive, or other sealing material used in sealing a lid wafer to a device wafer that contains a MEMS device, integrated circuit, or infrared detector. According to an embodiment of the present invention, an improved method for vacuum packaging such devices during fabrication is provided which substantially reduces disadvantages and problems associated with previously disclosed methods of vacuum packaging MEMS or similar devices. According to one embodiment of the present invention, there is provided a method for manufacturing lids and lid wafers for MEMS devices that comprises forming a trench between a sealing surface and a lid cavity whereby the trench is able to uptake the excess solder and prevent the solder from interfering with the operation of the MEMS or similar device.

The present invention provides various advantages over traditional lid manufacturing methods. It should be noted that any given embodiment may provide some, all, or none of these advantages. For example, because the trenches are created in the lid wafer prior to the separation of the individual vacuum-packaged MEMS devices, significant time and resources are conserved. Additionally, by providing a trench operable to uptake excess solder, the number of MEMS devices that are destroyed by the excess solder interfering with the operation of the MEMS devices is significantly reduced. This reduction in cost furthers the development of commercially-viable MEMS devices, by reducing the number of MEMS devices that malfunction. Other advantages may be readily ascertainable by those skilled in the art.

## BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings:

FIGURE 1 is a top view of a device wafer in accordance with an embodiment of the present invention;

FIGURE 2 is a partial cross-sectional view of a MEMS device in accordance with an embodiment of the present invention;

FIGURE 3 is a top view of a patterned side of a lid wafer in accordance with an embodiment of the present invention;

FIGURE 4 is an enlarged view of a portion of a lid wafer in accordance with an embodiment of the present invention;

5      FIGURE 5 is a partial cross-sectional view of the lid wafer of FIGURE 3;

FIGURE 6 is a partial cross-sectional view of the section of the lid wafer shown in FIGURE 4; and

FIGURE 7 is a partial cross-sectional view of a lid wafer and a device wafer illustrating the relationship of sealing layers on each wafer, in accordance with an embodiment of the present invention.

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#### DETAILED DESCRIPTION OF THE DRAWINGS

Infrared microelectromechanical systems (MEMS) devices, certain other inertial MEMS devices, and other similar devices require a vacuum environment to attain maximum performance. For example, infrared micro-bolometers require an operating pressure of less than 10 millitorr to minimize thermal transfer from the detector elements to the substrate and package walls. Thus, vacuum-compatible materials processes and equipment must be used. Infrared devices also require an optically-transparent cover. These packaging requirements result in high labor and capital expense and present a significant cost in producing commercially-viable MEMS devices. Under current techniques, MEMS devices packaging costs can be 10 to 100 times the basic device fabrication cost, even in reasonably high volume. Additionally, MEMS devices are fragile. According to various embodiments of the present invention, special handling techniques have been developed to protect the MEMS devices during the vacuum packaging of infrared detectors, integrated circuits, or MEMS devices. Generally, a plurality of MEMS or similar devices are packaged in individual vacuum- or hermetically-sealed packages simultaneously. The devices are created on a device wafer, which may have a silicon or other suitable substrate. The substrate may have sealing surfaces bondable to a lid wafer, which may be manufactured to have cavities or similar enclosures corresponding to each device on the device wafer. The lid wafer and device wafer are then bonded with each other, using solder, an adhesive or other suitable bonding material. After the lid wafer and device wafer are bonded, the result is a plurality of individually-

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packaged MEMS devices contained in one bonded wafer assembly. These individually-packaged devices may then be separated into individual devices by dicing, or sawing through the wafer assembly between the devices. During the manufacture of MEMS devices under previous methods, excess solder or adhesive from the sealing ring often  
5 overflowed into the device area, forming solder balls or spots that interfered with device operation. Additionally, solder leaked into the cavity area of the lid structure, thus obscuring the optical properties of the lid wafer and interfering with the circuits' operation, or destroying the circuit altogether.

One solution to high packaging costs is to eliminate traditional individual vacuum  
10 packaging of a completed die. This may be accomplished by moving the packaging step into the wafer fabrication area. A lid wafer is aligned and mounted to the device wafer, which has individual MEMS mounted thereon, using contiguous sealing layers disposed around each individual MEMS device on the device wafer. Unfortunately, MEMS devices manufactured according to this technique may result in an unacceptable number of MEMS  
15 devices being destroyed or having decreased performance. This destruction or decreased performance is due to the sealing material leaking onto the lid wafer enclosing each individual MEMS device. A solution to excess solder leaking into the area of the lid covering each individual MEMS device is to manufacture the lid wafer with a trench surrounding the area designed to cover the MEMS device. This trench may be formed on  
20 the lid wafer in such a way that the solder, adhesive, or other sealing material, which is forced out from between the sealing surfaces of the device wafer and the lid wafer during bonding, is retained therein. Thus excess solder, adhesive, or other bonding material is prohibited from entering the cavity area of the lid wafer.

Referring to FIG. 1, a silicon device wafer 10 is a standard substrate used for  
25 fabrication of integrated circuit devices, MEMS devices, or similar devices. However, any suitable substrate material may be used. For example, a substrate material with integrated circuit readout devices embedded therein may be used as the device wafer 10. Silicon device wafers may have many MEMS devices 12 formed thereon using traditional methods of integrated circuit fabrication. Although the embodiments disclosed herein  
30 discuss integrated circuit fabrication in terms of vacuum packaging for MEMS devices, the method may be used to provide vacuum packaging of any integrated circuit device, or similar device, formed on a substrate material and contained within a vacuum package.

Additionally, the method for manufacturing the lid wafer disclosed herein may be used in any vacuum or non-vacuum packaging of integrated circuit devices.

Each MEMS device 12 preferably has one or more associated bonding pads 14, which provide electrical connections to the MEMS device 12. As indicated in FIG. 1, each MEMS device 12 has two associated bonding pads 14. These bonding pads 14 are preferably disposed only on one side of the MEMS device 12. In any particular embodiment, however, bonding pads 14 may be disposed on any side, one side, or multiple sides of MEMS device 12. In addition to device wafer 10, MEMS devices 12, and bonding pads 14, FIG. 1 also depicts sealing surface 16 which defines the vacuum package around a MEMS device 12. Although this description discusses one MEMS device enclosed in each vacuum package, it should be noted that multiple MEMS devices may be enclosed within a vacuum package defined by sealing surface 16.

Referring now to FIG. 2, a single MEMS device 12 is illustrated to more completely show the layout on device wafer 10. A lead 18 connects each bonding pad 14 to MEMS device 12. A space is left between MEMS device 12 and bonding pad 14 to form the device sealing surface 16. Note that lead 18 runs beneath fabrication layers to be built within device sealing surface 16. Because the device sealing surface 16 defines the area of the device wafer 10 within which a vacuum package will be formed, leads 18 form electrical connections to bonding pads 14 without affecting the vacuums' seal existing around MEMS device 12.

Sealing surface 16 is formed on device wafer 10 such that a sealing layer 22 and bonding adhesion surface 24 may be formed thereon. Sealing layer 22 may be comprised of any suitable material having dielectric properties. Sealing layer 22 serves as a platform upon which bonding adhesion surface 24 may be deposited. Preferably, sealing layer 22 is composed of silicon nitride, although any suitable dielectric may be used. Sealing layer 22 provides electrical isolation for leads 18. A bonding adhesion surface 24 is fabricated on sealing layer 22 and may be fabricated using any combination of metal, metal alloy or other material that is suitable for bonding device wafer 10 and lid wafer 30 together. In one embodiment, bonding adhesion surface 24 may comprise a first layer of titanium, a second, middle layer of platinum, and a third layer of gold. However, there are many suitable materials or combinations of materials available for use in fabricating bonding adhesion surface 24. Bonding adhesion surface 24 may be deposited at the same time

bonding pads 14 are deposited on device wafer 10. Although device sealing surface 16 has been described as utilizing a heat-activated solder, a compression seal, such as indium compression seal, may also be used.

FIG. 3 illustrates a silicon lid wafer 30. Although the embodiment described below utilizes a silicon wafer as a substrate for the lid wafer 30, any suitable substrate material may be used. Lid wafer 30 includes a plurality of lid sealing surfaces 32 corresponding in number to the device sealing surfaces 16 on device wafer 10. Each of the lid sealing surfaces 32 is preferably a mirror image of the corresponding device sealing surface 16 so that lid wafer 30 mates with device wafer 10. Cavities 34 and bonding pad channels 36 are etched in the lid wafer 30 using an appropriate process such as wet or dry etching. Additionally, anisotropic etching using potassium hydroxide or any suitable basic solution may be used to etch cavities 34 and bonding pad channels 36. The etching process for cavities 34 and bonding pad channels 36 may include depositing a layer of silicon nitride, and patterning the silicon nitride layer to form an appropriate etch mask. Cavities 34 and bonding pad channel 36 provide clearance over the MEMS devices formed on device wafer 10 and the bonding pads 14 connected by leads 18 to MEMS device 12, respectively. Additionally, bonding pad channels 36 provide clearance over bonding pads 14 so that a dicing saw, etching process, or other suitable process may be used in a later step to open the lid wafer to expose the bonding pads for device testing before dicing of the wafer.

FIGURE 4 illustrates an individual sealing surface 32 and cavity 34. A trench 42 is fabricated within sealing surface 32 between bonding adhesion surface 38 and cavity 34. Bonding adhesion surface 38 is deposited on sealing surface 32, and is comprised of any combination of metal or metal alloys that will provide a surface wettable by the solder, adhesive, or other bonding material, and secure attachment to device wafer 10. In one embodiment, bonding adhesion surface 38 is preferably comprised of a first layer of titanium, followed by a second, middle layer of platinum, and a third, outer layer of gold.

FIGURE 5 illustrates a cross-sectional view of the lid wafer section illustrated by FIGURE 4. In the present embodiment, trench 42 is preferably disposed on sealing surface 32 between bonding adhesion surface 38 and cavity 34. Preferably, trench 42 is fabricated on lid wafer 30 during fabrication of bonding adhesion surface 38 and cavity 34. Trench 42 may be created in the same manner as the cavity 34 and bonding adhesion

surface 38 as well as bonding pad channels 36, by, for example, isotropic wet or dry etching, or anisotropic potassium hydroxide etching. In an embodiment using isotropic wet or dry etching to create trench 42, the trench may be formed with a depth determined by the width of the surface opening of the trench. Preferably, the depth of the trench is approximately equal to the width. In an embodiment using anisotropic etching into silicon surfaces, the depth is also determined by width of the surface opening. In anisotropic etching, the trench depth,  $D$ , may be determined by the equation  $2D \cong WTAN(54.74^\circ)$  where  $W$  is the width of the surface opening of the trench. It should be understood that the width and depth of trench 42 may be of any suitable dimensions so long as trench 42 provides the function of uptaking excess bonding adhesion material and preventing material from entering cavity 34. Additionally, a bonding layer 40 of solder or adhesive is preferably deposited on bonding adhesion surface 38. Thus, if a sealing material other than heat activated solder is used, the solder layer 40 may be replaced by a material necessary to obtain a vacuum or hermetic seal. In an alternative embodiment, an indium compression seal may be used.

Bonding layer 40 may be deposited using traditional integrated circuit fabrication techniques or other suitable deposition processes. For example, lid wafer 30 may be electroplated resulting in solder layer 40 being deposited upon lid bonding adhesion surface 38. Another method of depositing bonding layer 40, where a solder is used, includes using electroless plating. Another method of depositing bonding layer 40 includes using vacuum deposition. Yet another method of depositing bonding layer 40, where solder is used, includes using a pre-formed, pre-punched solder layer which is aligned over lid bonding adhesion surface 38 and attached thereto. Yet another embodiment uses solder balls deposited on bonding adhesion surface 38 using a template, which, when heated, form a uniform solder layer. Solder balls are then released from the template and attached to the bonding adhesion surface 38. The template is removed, leaving a relatively uniform distribution of solder balls on bonding adhesion surface 38. When lid wafer 30 is heated to an appropriate temperature, the solder balls melt and thus bond the lid wafer 30 to the device wafer 10 when the two wafers are pressed together.

Other suitable materials may be used to bond device wafer 10 to lid wafer 30, such as an indium compression seal, indium metal solder, metal alloy solder, or solder balls. Although the preferred embodiment contemplates depositing solder layer 40 on bonding



adhesion surface 38, bonding layer 40 may also be deposited on a bonding adhesion surface on device wafer 10 (not explicitly shown).

FIGURE 6 illustrates a cross section of lid wafer 30, and the relationship of lid cavities 34, bonding pad channels 36, sealing surfaces 32, bonding adhesion surfaces 38, bonding layer 40, and trenches 42, all with respect to lid wafer 30. Lid wafer 30, as illustrated in FIGURE 6, provides the basis for understanding the assembly illustrated by FIGURE 7. FIGURE 7 illustrates an assembly of a device wafer 10 and a lid wafer 30 ready for final assembly before placement in a vacuum furnace or other assembly chamber. Note that the lid wafer 30 is placed below the device wafer 10 so that the bonding layer 40 faces upward. Device wafer 10 is then aligned over lid wafer 30 such that the bonding adhesion surfaces 24 on device wafer 10 are aligned directly over the corresponding bonding adhesion surface 38 and bonding layer 40 on lid wafer 30. Upon heating of the bonding layer 40, device wafer 10 and lid wafer 30 are bonded together such that all MEMS devices 12 on device wafer 10 are enclosed in a package. If bonding layer 40 is not heat-activated, any other suitable chamber such as a vacuum chamber may be used in place of a heating chamber or vacuum furnace to provide the appropriate environment for bonding.

When device wafer 10 is brought into contact with lid wafer 30, some of the material of bonding layer 40, such as solder, adhesive, or other bonding material, may drip or ooze toward lid cavity 34. Trench 42 is disposed between bonding adhesion layer 38 on sealing layer 32 to prevent this material from entering lid cavity 34. During the use of solder balls to mate lid wafer 30 with device wafer 10, some of the solder balls may inadvertently become unattached from bonding adhesion surface 38 and roll toward lid cavity 34. In such a case, trench 42 is operable to retain these solder balls before they reach lid cavity 34 and are melted to lid wafer 30. Additionally, if some of the solder balls are not fully melted upon heat application to the assembly, the subsequent dicing of each individually packaged MEMS device could cause the solder balls to become detached and free-roaming within each individual package. If some of the solder balls enter the cavity, the solder balls could interfere with or even destroy MEMS device 12 by interfering with the electrical properties therein upon the application of electromagnetic energy. Thus, trench 42 is operable to prevent these solder balls from entering lid cavity 34.

Although the present invention has been described in detail, it should be understood that various changes, substitutions, and alterations may be made, without departing from the spirit and scope of the present invention as defined by the claims.

WHAT IS CLAIMED IS:

1. A method for manufacturing an integrated circuit device lid, comprising the steps of:
  - forming one or more a lid cavities on the surface of a lid wafer;
  - 5 forming one or more sealing surfaces on the lid wafer disposed around the cavity;
  - and
  - forming one or more trenches in the lid wafer, wherein each trench is disposed between one of the sealing surfaces and one of the lid cavities.
- 10 2. The method of Claim 1, wherein the one or more lid cavities are formed by wet or dry isotropic etching.
3. The method of Claim 1, wherein the step of forming one or more lid cavities comprises forming a plurality of lid cavities on the surface of the lid wafer.
- 15 4. The method of Claim 3, wherein the step of forming one or more sealing surfaces comprises forming a plurality of sealing surfaces on the surface of the lid wafer, each sealing surface disposed around one of the plurality of lid cavities.
- 20 5. The method of Claim 4, wherein the step of forming one or more trenches comprises forming a plurality of trenches, each trench disposed between one of the sealing surfaces and one of the lid cavities.
6. The method of Claim 1, wherein the one or more trenches are formed by
- 25 isotropic wet or dry etching.
7. The method of Claim 1, wherein the one or more trenches are formed by anisotropic etching.

8. The method of Claim 1, wherein the steps of forming one or more lid cavities and one or more sealing surfaces disposed around the cavity comprise bonding a window wafer to the lid wafer, wherein the window wafer is preformed with one or more cavities and one or more sealing surfaces.

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9. The method of Claim 1, wherein the one or more trenches are each formed with a depth and width that are approximately equal.

10. The method of Claim 1, wherein the depth of each of the one or more trenches is determined by the width of a surface opening of the trench.

11. A lid for an integrated circuit device comprising:  
a lid wafer;  
at least one cavity formed in the lid wafer;  
15 at least one sealing structure disposed around the cavity for sealing the lid wafer to a device wafer;

at least one at least substantially continuous trench disposed around one of the at least one cavities and between the cavity and the sealing structure, wherein the trench is operable to uptake excess material of the sealing structure and prevent any material of the  
20 sealing structure from entering the cavity.

12. The lid of Claim 11, wherein the at least one cavity comprises a plurality of cavities, each cavity surrounded by one of the at least one sealing structures.

25 13. The lid of Claim 12, wherein one of the at least one trenches is disposed between each sealing structure and corresponding cavity.

14. The lid of Claim 11, wherein the sealing structure is a solder layer.

30 15. The lid of Claim 11, wherein the sealing structure is an adhesive.

16. The lid of Claim 11, wherein the sealing structure is an indium compression seal.

17. A lid for an integrated circuit device comprising:  
5 a lid wafer;  
a cavity formed in the lid wafer;  
a sealing structure disposed around the cavity for sealing the lid wafer to the device wafer; and  
an at least substantially continuous retaining structure disposed around the cavity  
10 and between the cavity and the sealing structure for retaining excess material of the sealing structure and preventing the material of the sealing structure from entering the cavity.

18. The lid of Claim 17, wherein the retaining structure is disposed between the  
15 sealing structure and the cavity.

19. A lid for an integrated circuit device, comprising:  
a lid wafer, having one or more lid cavities on the surface thereof; and  
one or more sealing surfaces on the lid wafer disposed around the one or more  
20 cavities wherein the lid wafer has one or more at least substantially continuous trenches formed therein, and wherein each trench is disposed around one of the lid cavities and between that lid cavity and one of the sealing surfaces.

20. The lid of Claim 19, wherein the one or more lid cavities comprises a  
25 plurality of lid cavities.

21. The lid of Claim 19, wherein the one or more sealing surfaces comprises a plurality of sealing surfaces.

22. The lid of Claim 19, wherein the one or more trenches comprises a plurality  
30 of trenches.

23. The lid of Claim 19, wherein the lid wafer comprises a window wafer, the window wafer being preformed with the one or more cavities and the one or more sealing surfaces.

5        24. The lid of Claim 19, wherein the one or more trenches each have a depth and width that are approximately equal.

25. The lid of Claim 19, wherein the depth of each of the one or more trenches corresponds to the width of a surface opening of the trench.

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26. The lid of Claim 11, wherein the one or more cavities are formed by wet or dry isotropic etching.

15        27. The lid of Claim 11, wherein the at least one trenches are formed by wet or dry isotropic etching.

28. The lid of Claim 11, wherein the at least one trenches have a depth and width that are approximately equal.

20        29. The lid of Claim 11, wherein the depth of each of the at least one trenches is determined by the width of a surface opening of each of the at least one trenches.

25        30. The lid of Claim 11, wherein the each of the at least one cavities formed in the lid wafer is operable to receive an integrated circuit device such that at least a portion of the integrated circuit device extends into the cavity.

31. The lid of Claim 11, wherein the each of the at least one cavities formed in the lid wafer is operable to receive a microelectromechanical systems (MEMS) device such that at least a portion of the MEMS device extends into the cavity.

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FIG. 1

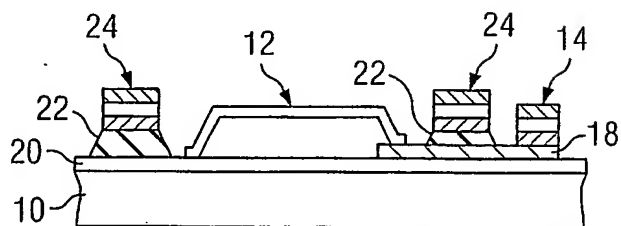
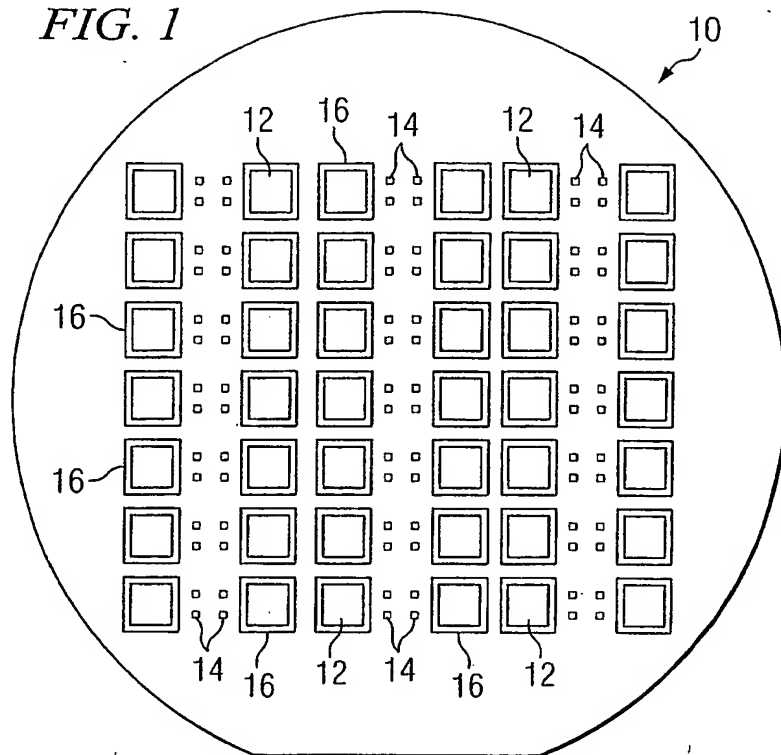


FIG. 2

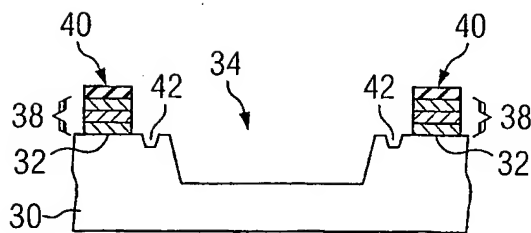
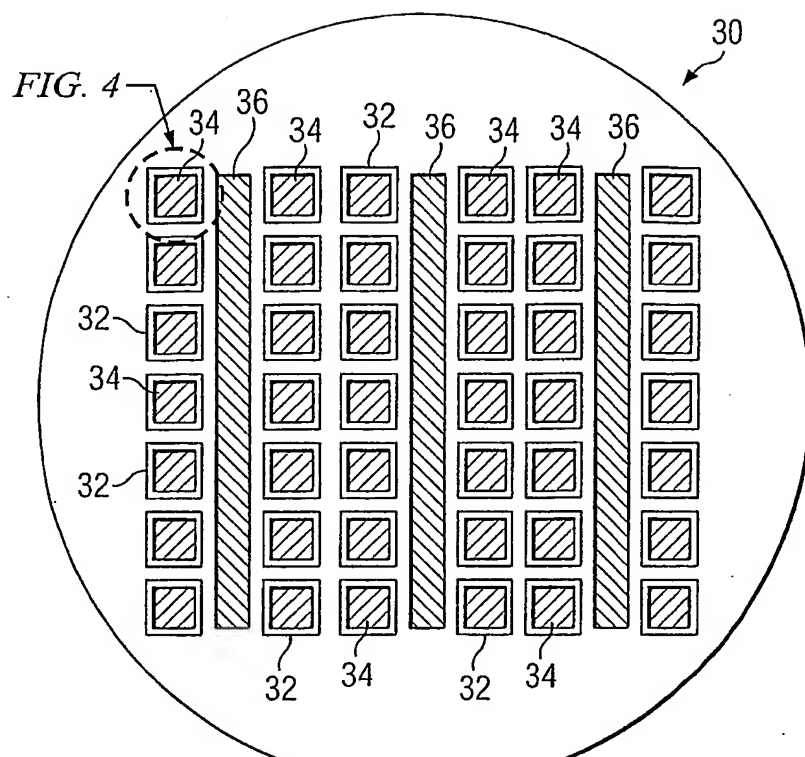
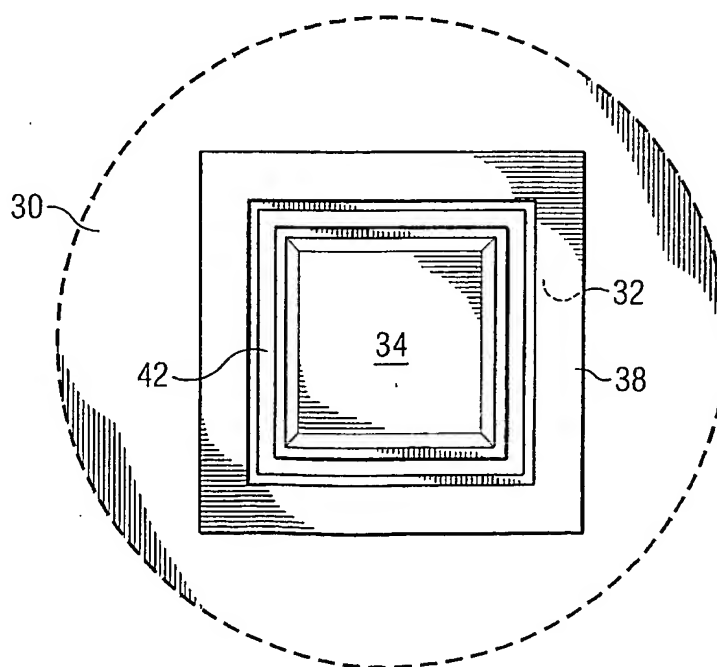


FIG. 5

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*FIG. 3*



*FIG. 4*



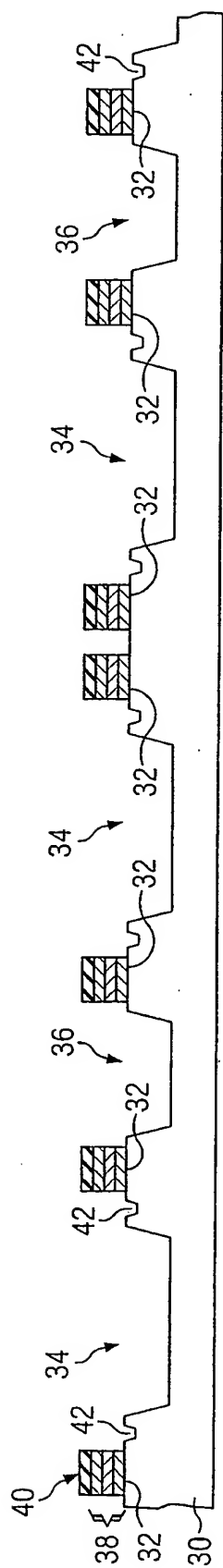


FIG. 6

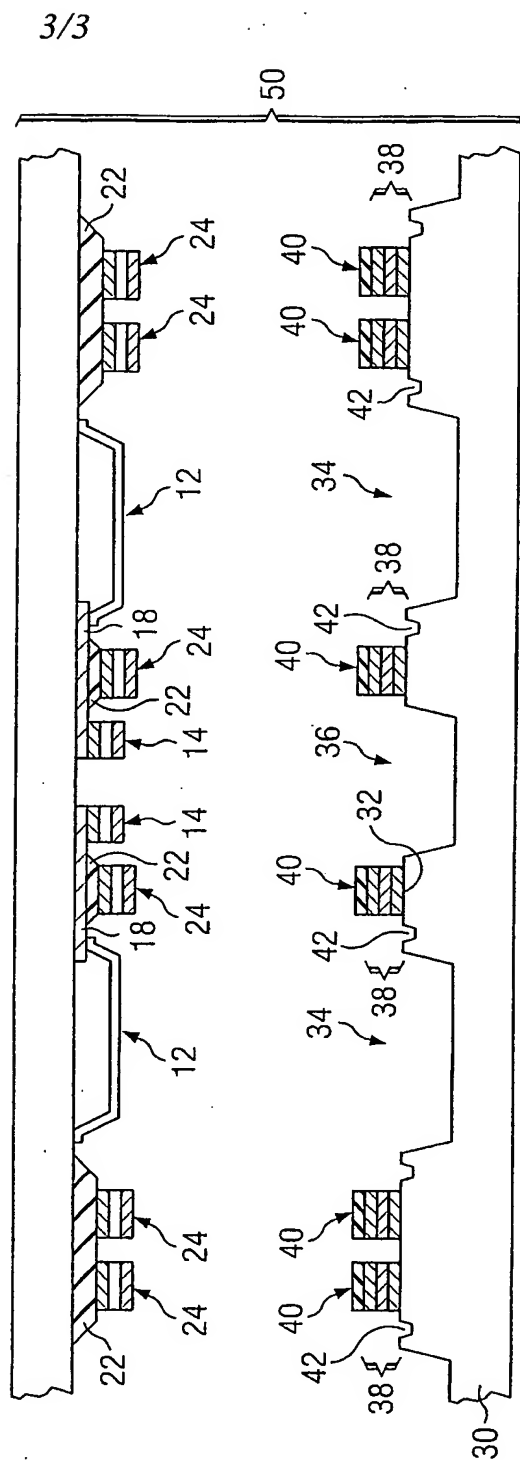


FIG. 7

# INTERNATIONAL SEARCH REPORT

International Application No  
'US2004/012131

**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 B81B7/00

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
IPC 7 B81B H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/106862 A1 (JORDAN LARRY L ET AL) 8 August 2002 (2002-08-08)  abstract; figures 1-3 page 2, paragraph 14 - page 4, paragraph 23	1-5,7, 9-13,15, 17-22, 24-26, 28-31
A	claims 1-13	6,27
X	EP 0 794 558 A (FORD MOTOR CO) 10 September 1997 (1997-09-10) abstract; figures 1-5	1,19
X	US 5 388 443 A (MANAKA JUNJI) 14 February 1995 (1995-02-14) abstract; figures 4,5	1,19

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

\* Special categories of cited documents:

\*A\* document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search

8 September 2004

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15/09/2004

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# INTERNATIONAL SEARCH REPORT

ional Application No

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Patent document cited in search report		Publication date	Patent family member(s)		Publication date
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US 5388443	A	14-02-1995	NONE		